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(54) Title: DATA PROCESSING METHOD AND DEVICE

(57) Abstract: The invention relates to a method of simultaneously operating a sequential processor and a reconfigurable array wherein data are transferred into said reconfigurable array from a data cache to said array and wherein results produced in said array from said data are written to a destination.

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# INTERNATIONAL SEARCH REPORT

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**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 G06F15/78

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

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**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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X	<p>HAUSER J R ET AL: "Garp: a MIPS processor with a reconfigurable coprocessor" FIELD-PROGRAMMABLE CUSTOM COMPUTING MACHINES, 1997. PROCEEDINGS., THE 5TH ANNUAL IEEE SYMPOSIUM ON NAPA VALLEY, CA, USA 16-18 APRIL 1997, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 16 April 1997 (1997-04-16), pages 12-21, XP010247463 ISBN: 0-8186-8159-4 page 12, right-hand column, line 6 - page 13, left-hand column, line 1 ----- -/--</p>	1-7

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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